REMARKS

Present Status of the Application

Claims 1-12 remain pending in the application. The Final Office Action dated January 15, 2003 rejected all the pending claims 1-12 under 35 USC 103(a) as being unpatentable over Egawa et al. (US Patent No. 6,376,278) in view of Belke Jr. et al. (US Patent No. 6,326,241) and Hung (US Patent No. 6,380,624).

The Applicant has most respectfully considered the remarks set forth in the Office Actions. In this response, claims 1 and 7 have been amended to patently distinguish over the prior art references. No claims have been deleted and no new matter has been introduced in the amendments made.

In view of the above amendments and following remarks, reconsideration and allowance of the claims are respectfully requested.

Discussion of rejection under 35 USC 103

The final Office Action rejected claims 1-12 under 35 USC 103(a) as being allegedly unpatentable over Egawa et al. in view of Belke Jr. et al. and Hung. In consideration of amended claims 1 and 7, this rejection is respectfully traversed.

As recited in amended claims 1 and 7, each of the substrates to be mounted on the single wafer includes *a plurality of package units, each package units corresponding to one chip of the wafer*. As a result, when the substrates are mounted on the wafer, a plurality of chips are simultaneously assembled (which reduces the process time), and the gaps between the substrates further allow favorable filling of the underfill material.

None of the relied prior art references adequately teach or suggest the mount of substrates constructed as above.

The prior art, in reference to Egawa et al., teaches a manufacturing process of flip chip packages in which, as illustrated in FIG. 2(A) through FIG. 2(C), each wiring substrate 28 corresponds to a single chip 18. Clearly, this wiring substrate 28 of the prior art does not meet the claim limitation wherein *each substrate integrates a plurality of package units, each package unit corresponding to one chip.* Moreover, each wiring substrate 28 is mounted to one individual chip 18 **after** the wafer 10 is diced into separated chips 18, which is contradictory to the teachings of the claimed invention.

It is noted that Egawa et al. further discloses a variant assembly process in which, as illustrated in FIG. 8(A) through FIG. 8(C), a single substrate 62 including a plurality of device regions 66 is mounted on the wafer 10. This teaching is also deficient to meet the claim limitation wherein *a plurality of substrates, each respectively including a plurality of packaging units, are mounted on the wafer with a gap separating two adjacent substrates*, as recited in the claims.

Applicant respectfully points out that it is improper to select and combine parallel and non-coexistent process steps from Egawa's embodiments, since the proposed modification would destroy primary advantages of the respective embodiments. The Office Action is urged to avoid the temptation of using the claims as a blueprint to pick and choose isolated features from the reference to achieve the claimed combination.

Belke Jr. et al. is relied upon for teaching the provision of a plurality of bonding pads on the substrate, and the formation of bumps on the bonding pads. Furthermore, Hung is relied upon

for teaching the construction of the substrates, including patterned copper films alternately laminated with insulating layers.

It is noted that none of the above secondary references adequately teach, suggest or motivate the claimed invention wherein "*a plurality of substrates are mounted on a wafer, each substrate including a plurality of packaging units respectively corresponding to the chips of the wafer*". Therefore, even if they are combined with one another, it is submitted that none of the relied references adequately teach or suggest all the claim limitations as emphasized above.

For at least the above reasons, it is submitted that claims 1 and 7 and thereon-depended claims 2-6 and 8-12 patently distinguish over the prior art references, and withdrawal of the obviousness rejection is respectfully solicited.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-12 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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